

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-10 (canceled)

Claim 11 (previously presented): A delay circuit applied to a synchronizing circuit comprising:

a first delay line which includes unit delay elements and transfers a forward pulse signal;

a second delay line which includes unit delay elements and transfers a backward pulse signal; and

a state holding section which is brought into a set state or a reset state according to a transfer position of the forward pulse signal transferred along said first delay line and said backward pulse signal transferred along said second delay line in the set state and a clock signal along said second delay line in the reset state,

wherein each of said unit delay elements constituting said first and second delay lines includes:

a clocked inverter circuit to which a first pulse signal corresponding to one of said forward and backward pulse signals output from a preceding delay unit is supplied, said clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.

Claim 12 (previously presented): The delay circuit according to claim 11, wherein said logic circuit is a NOR circuit and said clocked inverter circuit delays a trailing edge of said first pulse signal.

Claim 13 (previously presented): The delay circuit according to claim 11, wherein said logic circuit is a NAND circuit and said clocked inverter circuit delays a leading edge of said first pulse signal.

Claim 14 (previously presented): The delay circuit according to claim 11, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor, and at least one of a channel width, channel length, threshold voltage and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage and substrate voltage of the PMOS transistor.

Claim 15 (previously presented): The delay circuit according to claim 14, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set at a value other than one and a rise time of said first pulse signal is made different from the decay time of said first pulse signal.

Claims 16-20 (canceled)

### REMARKS/ARGUMENTS

The final office action of August 22, 2003 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-20 remain in this application. Claims 1-10 and 16-20 have been canceled without prejudice or disclaimer.

Preliminarily, applicants note with appreciation the indication that the application contains allowable subject matter. Specifically, claims 11-15 have been allowed.

Claims 1, 2, 6, 7, and 16-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent no. 5,319,253 to You. Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over You. Claims 4, 5 and 8-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over You in view of U.S. patent no. 5,605,270 to D'Souza et al. Also, claim 20 has been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent no. 5,723,993 to Cha. Applicants respectfully traverse these rejections. Nonetheless, in order to expedite prosecution, Applicants have canceled the rejected claims. Applicants reserve the right to pursue the canceled claims in a continuation application. In view of the cancellation of all rejected claims (1-10 and 16-20), the rejections are now moot and Applicants respectfully request withdrawal of the rejections.

### CONCLUSION

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

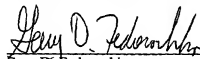
All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

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